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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/884,675 | 06/19/2001 | Matthew H. Reilly | 1662-38200 JMH (P00-3546) | 3217 |
| 22879 | 7590 | 12/28/2004 | EXAMINER | |
| HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400 | | | HARKNESS, CHARLES A | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2183 | |

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/884,675

Applicant(s)

REILLY ET AL.

Examiner

Charles A Harkness

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25, 27, 28, 32 and 35-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11, 12, 19, 22, 24, 27, 28, 32 and 35-37 is/are allowed.
- 6) ☒ Claim(s) 1-10, 13-18, 20-21, 23 and 25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the amendment to the title, the objection of the specification has been withdrawn.
2. In response to the amendment to claims 11 and 27, the objections of claims 11 and 27 have been withdrawn.
3. In response to the amendment to claims 11-12, 19, 22, 24, 27-28, and 32, the objections of claims 11-12, 19, 22, 24, 27-28, and 32 have been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 13-18, 20-21, 23, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Adler et al., U.S. Patent Number 5,634,023 (herein referred to as Adler).
5. Referring to claim 1 Adler has taught a processor, comprising:
 - a first exception handler that receives and handles critical excepted instructions (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is speculative, thus performance critical, the speculative handler sets a semaphore); and
 - a second exception handler that receives and handles non-critical excepted instructions (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception).

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6. Referring to claim 2 Adler has taught wherein the critical excepted instructions comprise exceptions that are performance critical (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is speculative, thus performance critical, the speculative handler sets a semaphore).

7. Referring to claim 3 Adler has taught wherein the non-critical excepted instructions comprise exceptions that are not performance critical (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception).

8. Referring to claim 13 Adler has taught wherein the second exception handler operates non-speculatively (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception; the error handler only receives instruction exceptions when the code is to be committed).

9. Referring to claim 14 Adler has taught wherein the second exception handler causes non-critical excepted instructions to be resolved only when it is certain that the excepted instruction is in an executing program (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception; the error handler only receives instruction exceptions when the code is to be committed).

10. Referring to claim 15 Adler has taught further comprising a plurality of pipelines with multiple stages, and wherein excepted instructions may arise in one or more of the pipeline stages (Alder figure 4 column 1 lines 23-40).

11. Referring to claim 16 Adler has taught wherein excepted instructions arising from said one or more pipeline stages is routed to the first exception handler or second exception handler based on a predetermined criteria (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the

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exception is non-speculative, thus not performance critical, an error handler handles the specific exception; these criteria are predetermined).

12. Referring to claim 17 Adler has taught wherein the predetermined performance criteria relates to performance of the processor (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception).

13. Referring to claim 18 Adler has taught an exception handler for a processor that resolves excepted instructions, comprising:

a speculative exception handler that receives critical excepted instructions and resolves said critical excepted instructions on a speculative basis (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is speculative, thus performance critical, the speculative handler sets a semaphore; the speculative basis is interpreted to mean that it handles speculative instructions in a certain manner; the system then resolves the exception once the speculative instruction is to be committed); and

a non-speculative exception handler that receives non-critical excepted instructions and resolves said non-critical excepted instructions on a non-speculative basis (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception).

14. Referring to claim 20 Adler has taught wherein the non-speculative exception handler delays resolution of said non-critical excepted instructions until it is certain that said non-critical excepted instruction lies in an actual path of an executing program (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an

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error handler handles the specific exception; the error handler only receives instruction exceptions when the code is to be committed).

15. Referring to claim 21 Adler has taught a processor, comprising:

at least one pipeline with a plurality of stages (Adler figure 4 column 1 lines 23-40);
an algorithm for detecting non-executable instructions in said at least one pipeline, wherein said algorithm generates a command that identifies the non-executable instruction and identifies a reason that the non-executable instruction will not execute (Adler abstract, figure 3 and 6, column 6 lines 28-60);

a speculative exception handler that receives said command for any non-executable instructions that are critical to processor performance (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is speculative, thus performance critical, the speculative handler sets a semaphore; the speculative basis is interpreted to mean that it handles speculative instructions in a certain manner; the system then resolves the exception once the speculative instruction is to be committed); and

a non-speculative exception handler that receives said command for any non-executable instructions that are not critical to processor performance (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception).

16. Referring to claim 23 Adler has taught wherein the non-speculative exception handler delays resolution of said non-critical non-executable instructions until it is certain that a non-critical non-executable instruction lies in an actual path of an executing program (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance

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critical, an error handler handles the specific exception; the error handler only receives instruction exceptions when the code is to be committed).

17. Referring to claim 25 Adler has taught wherein said non-speculative exception handler includes logic for resolving non-critical non-executable instructions (Adler abstract, figure 3 and 6, column 6 lines 28-60; if the exception is non-speculative, thus not performance critical, an error handler handles the specific exception; the error handler only receives instruction exceptions when the code is to be committed).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adler in view of Le et al., U.S. Patent Number 6,721,874 (herein referred to as Le).

19. Referring to claim 4 Adler has not taught wherein the critical excepted instructions include branch mispredictions. Le has taught wherein the critical excepted instructions include branch mispredictions (Le column 8 lines 23-41). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the

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time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

20. Referring to claim 6 Adler has not taught wherein the critical excepted instructions include jump mispredictions. Le has taught wherein the critical excepted instructions include jump mispredictions (Le column 8 lines 23-41). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

21. Claims 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adler in view of Safford et al., U.S. Patent Number 6,681,322 (herein referred to as Safford).

22. Referring to claim 7 Adler has not taught wherein the non-critical excepted instructions include illegal instructions. Safford has taught wherein the non-critical excepted instructions include illegal instructions (Safford column 1 lines 49-61). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

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23. Referring to claim 9 Adler has not taught wherein the non-critical excepted instructions include invalid instructions. Safford has taught wherein the non-critical excepted instructions include invalid instructions (Safford column 1 lines 49-61). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

24. Referring to claim 10 Adler has not taught wherein the excepted instructions include arithmetic overflows. Safford has taught wherein the excepted instructions include arithmetic overflows (Safford column 1 lines 49-61). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

25. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adler in view of Rahman et al., U.S. Patent Number 5,7654,007 (herein referred to as Rahman).

26. Referring to claim 8 Adler has not taught wherein the non-critical excepted instructions include cache parity errors. Rahman has taught wherein the non-critical excepted instructions include cache parity errors (Rahman column 19 lines 52-57). Adler has not given an exclusive

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list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

27. Referring to claim 5 Adler has not taught wherein the critical excepted instructions include load/store traps. Rahman has taught wherein the critical excepted instructions include load/store traps (Rahman column 19 lines 52-57). Adler has not given an exclusive list of exceptions that the system checks for. However, one of ordinary skill in the art would recognize that a system would want to check for particular exception to prevent the system from producing incorrect results. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include particular exceptions in the exceptions that the system of Adler checks for to prevent the system from producing incorrect results.

Allowable Subject Matter

28. Claims 11-12, 19, 22, 24, 27-28, 32 and 35-37 are allowed.

29. Referring to claims 11-12, 19, 22, 24, 27-28, 32 and 35-37, the limitations include the exception handler executing in a speculative manner, where speculative operation is known to by executing even though (an) instruction(s) that cause the critical exception may not be in the an actual program path.

Response to Arguments

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30. Applicant's arguments filed 09/17/04 have been fully considered but they are not persuasive.

31. In the remarks, Applicant argues in essence that:

“Adler is directed to a ‘software mechanism for accurately handling exceptions generated by speculatively scheduled instructions.’”

And

“Rather than dealing with hardware based mechanisms for speculative scheduling of instructions, Adler deals with speculative scheduling by a compiler at compile time.”

32. This is not persuasive. Applicant does not limit in his claims that the exception handler(s) are performed in hardware, and does not make any mention of where the exception handlers are not to be implemented in software. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., exception handlers are not to be implemented in software) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

33. Also, it is well known in the art that exception handlers are actually a piece of software that is executed by the processor; that is the reason that the processor ‘loads’ an exception handler, and must flush the pipeline with the current instruction when an exception occurs.

34. In addition, the functionality of hardware and software in digital computing are logically the same. Both operate using bits that can be “on” or “off”, in combination with logic, to compute values. Although they are physically different, and have different advantages and drawbacks, since anything that can be implemented in hardware can be implemented in software, it

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would be an obvious change to implement certain logic in software versus hardware to reduce costs of physical computer chips.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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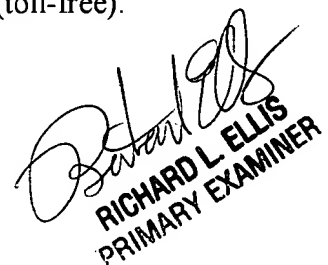
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Charles Allen Harkness

Patent Examiner

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December 20, 2004



RICHARD L. ELLIS
PRIMARY EXAMINER